IN THE CLAIMS

Please amend the claims as follows.

1. - 9. (Canceled)

10. (Previously Presented) An integrated circuit comprising:

a plurality of input nodes;

a plurality of output nodes;

a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits;

a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits; and

a controller to configure the register circuits based on a result from the logic function of the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals.

11. (Original) The integrated circuit of claim 10, wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

12. (Original) The integrated circuit of claim 11, wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines.

13. (Original) The integrated circuit of claim 12, wherein the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit.

14. (Previously Presented) An integrated circuit comprising:

a plurality of input nodes to receive a plurality of input bits;

a plurality of output nodes to provide a plurality of output bits;

a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes, each of the register circuits including a number of register cells, the number of register cells equaled to 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit, each of the register circuits further including a select circuit connected to a subset of the number of register cells through a number of select lines, the number of select lines equaled to a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit;

a logic circuit connected to the register circuits to perform a logic function on a plurality of bits held by the register circuits, wherein the logic circuit includes:

a calculation unit to perform the logic function on a plurality of bits;

a plurality of memory units to store results from the logic function;

a counter to count values stored in the memory units;

a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells; and

a controller to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned by one or more bit time intervals.

15. (Previously Presented) The integrated circuit of claim 10, wherein the logic circuit is configured to perform an OR function.

16. (Original) The integrated circuit of claim 14, wherein the memory units are arranged in rows and columns, wherein the memory units in the same row form a shift register.

17. (Original) The integrated circuit of claim 14, wherein the counter includes a plurality of counter memory units, each of the counter memory units being connected to one shift register.

18. (Original) A system comprising:

a parallel bus including a plurality of bus lines to carry a plurality of bits on each of the bus lines; and

a first integrated circuit including a plurality of register circuits, each of the register circuits being connected to one of the bus lines, and each of the register circuits including,

a shift register connected to an input node, the shift register including a plurality of register cells,

a select circuit connected to a subset of the number of register cells through a number of select lines, the select circuit including an output node, and

a controller connected to the select circuit and the register cells to configure the register cells to select only one of the select lines to be a part of a conductive path connected between the input node and the select circuit output node.

19. (Original) The system of claim 18 further comprising a second integrated circuit connected to the parallel bus.

20. (Original) The system of claim 19, wherein the parallel bus is formed on a circuit board, and the first and second integrated circuits are located in the circuit board.

21. (Original) The system of claim 19 further comprising:

a first circuit board, wherein the parallel bus is formed on the first circuit board and the first integrated circuit is located on the first circuit board; and

a second circuit board, wherein the second integrated circuit is located on the second circuit board, the second circuit board being inserted into a bus slot that connects to the parallel bus.

22. (Original) The system of claim 19, wherein the first and second integrated circuits are located on separate circuit boards, and the parallel bus is not formed on the first or second circuit boards.

23. - 30. (Canceled)

31. (Previously Presented) A method comprising:

receiving a plurality of input bits at a plurality of input nodes of a plurality of register circuits;

providing a plurality of output bits at a plurality of output nodes of the register circuits;

performing a logic function on a plurality of bits held by the register circuits to produce a rotation number; and

aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, based on the rotation number, when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval.

32. (Previously Presented) The method of claim 31, wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the register circuits.

33. (Previously Presented) The method of claim 32, wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines.

34. (Previously Presented) The method of claim 33, wherein the number of select lines equals a maximum number of bit time intervals of misalignment of a parallel bus that connects to the register circuits.

35. (Canceled)